What is claimed is:

1. A process, comprising:

forming a first dielectric layer on a substrate;

patterning the first dielectric layer such that a plurality of vertically oriented posts are formed, the post having a top surface;

forming a second dielectric layer over and adjacent to the posts, the second dielectric layer having a top surface; and

polishing the second dielectric layer such that its top surface is substantially even with the top surfaces of the posts.

2. The process of Claim 1, wherein the substrate comprises a dielectric material.

3. The process of Claim 1, wherein the substrate is a material selected from the group consisting of silicon carbide, silicon nitride, and carbon doped oxides of silicon.

4. The process of Claim 1, further comprising curing the second dielectric layer.

5. The process of Claim 1, further comprising aging the second dielectric layer.

6. The process of Claim 1, further comprising forming dual damascene

openings in the second dielectric layer.

7. The process of Claim 1, wherein forming the first dielectric layer comprises depositing an oxide of silicon.

8. The process of Claim 7, wherein forming the second dielectric layer comprises chemical vapor deposition of a low-k material.

9. The process of Claim 7, wherein forming the second dielectric layer comprises spinning on a low-k material.

10. The process of Claim 1, wherein the second dielectric has a lower dielectric constant than the first dielectric.

11. A dielectric structure, comprising:

a plurality of posts disposed on a substrate, the posts comprising an electrically non-conductive material; and

a low-k dielectric material disposed around the posts.

12. The dielectric structure of Claim 11, wherein the substrate comprises a material selected from the group consisting of silicon carbide, silicon nitride, and carbon doped oxides of silicon.

13. The dielectric structure of Claim 11, wherein the posts are vertically oriented and comprised of an oxide of silicon.

14. The dielectric structure of Claim 13, wherein the oxide of silicon is a fluorine doped oxide.

15. The dielectric structure of Claim 13, wherein the posts have a rectangular base.

16. An integrated circuit, comprising:

a substrate having interconnected electrical elements therein;

a first dielectric layer disposed over the substrate;

at least one electrically non-conductive, vertically oriented post disposed on the first dielectric layer; and

a second dielectric layer disposed on the first dielectric layer such that the second dielectric surrounds the at least one post.

17. The integrated circuit of Claim 16, wherein the second dielectric layers has trenches therein.

18. The integrated circuit of Claim 17, further comprising metal disposed in the trenches.

19. The integrated circuit of Claim 18, wherein the metal comprises copper.

20. An integrated circuit, comprising:

a substrate having interconnected electrical elements therein;

a first dielectric layer disposed over the substrate;

a plurality of electrically insulating structures disposed on the first dielectric layer; and

a second dielectric layer disposed on the first dielectric layer such that the second dielectric surrounds the plurality of structures.

21. The integrated circuit of Claim 20,wherein the structures are identical.

22. The integrated circuit of Claim 20, further comprising metal filled damascene trenches in the second dielectric layer.

23. The integrated circuit of Claim 20, wherein the structures are comprised of an oxide of silicon, and the second dielectric layer is comprised of a porous material having a dielectric constant lower than that of silicon dioxide.

24. A process, comprising:

depositing a silicon nitride layer on a wafer;

depositing an insulating layer over the silicon nitride layer;

patterning the insulating layer such that a plurality of structures are

formed, the structures each having a top surface;

depositing a porous dielectric material over and adjacent to the structures, the porous dielectric material having a void fraction; and

polishing the porous dielectric material such that a top surface thereof is substantially even with the top surfaces of the structures;

treating the porous dielectric material such that its void fraction is increased.

25. The integrated circuit of Claim 24, wherein the porous dielectric material has a lower dielectric constant than that of the structures.